WHAT IS CLAIMED IS:

1. A transconductance cell for use in a system on chip to reduce adverse effects of bulk semiconductor voltages on transconductance comprising a plurality of current sources interconnected to provide an output transconductance control voltage, and a variable load for the current sources including first and second load resistors each serially connected with one of the plurality of current sources, and a variable resistance interconnecting nodes of the load resistors, the variable resistance comprising a pair of native MOS transistors having low threshold voltages.

2. The transconductance cell as defined by claim 1 wherein the first and second load resistors comprise first and second MOS transistors.

3. The transconductance cell as defined by claim 2 wherein the pair of native transistors are serially connected between source elements of the first and second MOS transistors.

4. The transconductance cell as defined by claim 3 wherein gate elements of the native MOS transistors are connected to receive a control voltage.

5. The transconductance cell as defined by claim 4 wherein the system on chip comprises a radio receiver, and the transconductance cell is used in a low pass filter of the radio receiver.

6. The transconductance cell as defined by claim 5 wherein the transconductance cell is used also in a voltage controlled oscillator.

7. The transconductance cell as defined by claim 4 wherein the system on a chip comprises a radio receiver, andtransconductance cell is used in a voltage controlled oscillator.

8. The transconductance cell as defined by claim 1 wherein the system on a chip comprises a radio receiver, the transconductance cell is used in a low pass filter of the radio receiver.

9. The transconductance cell as defined by claim 8 wherein the tranconductance cell is used also in a voltage controlled oscillator.

10. The transconductance cell as defined by claim 1 wherein the system on chip comprises a radio receiver, and a transconductance cell is used in a voltage controlled oscillator.

11. A method of reducing noise susceptibility due to bulk semiconductor voltages in a system on chip employing gyrators in filter elements comprising the steps of:

a) providing a gyrator cell with resistive loads for a plurality of current sources, the resistive loads including first and second MOS transistors, and

b) connecting a variable resistance between the first and second MOS transistors, the variable resistance comprising two serially connected native MOS transistors having low threshold voltages.

12. The method as defined by claim 11 wherein gate elements of the native MOS transistors are connected to receive a control voltage.

13. The method as defined by claim 12 wherein the system on the chip comprises a radio receiver, and wherein gyrators are used in low pass filters of the radio receiver.

14. A gyrator comprising a plurality of current sources interconnected to provide output transconductance control voltages, and a variable load for the current sources including first and second load resistors, each serially connected with one of the plurality of current sources, and a variable resistance interconnecting nodes of the load resistors, the variable transistor resistance comprising a pair of native MOS transistors having low threshold voltages.

15. The gyrator as defined by claim 14 wherein the first and second load resistors comprise first and second MOS transistors.

16. The gyrator as defined by claim 14 wherein the pair of native transistors are serially connected between source elements of the first and second MOS transistors.

17. The gyrator as defined by claim 16 wherein gate elements of the native MOS transistors are connected to receive a control voltage.

ADD 7